Quad 40V/1A Step-Down Switching Regulator with 100% Duty Cycle Operation

FEATURES

- **Wide Input Range: 3.2V to 40V**
- **Four 1A Outputs**
- **100% Duty Cycle Operation**
- **Resistor-Programmed Constant Frequency**
- Short-Circuit Robust
- Wide SYNC Range: 350kHz to 2.2MHz
- Anti-Phase Switching Reduces Ripple
- 800mV FB Voltage
- Independent Run/Soft-Start Pins
- Shutdown with UVLO
- Internal Compensation
- Thermal Shutdown
- Tiny 28-Lead (4mm × 5mm) Thermally Enhanced QFN Package

APPLICATIONS

- Automotive Battery Regulation
- Industrial Control Supplies
- Wall Transformer Regulation
- Distributed Supply Regulation

DESCRIPTION

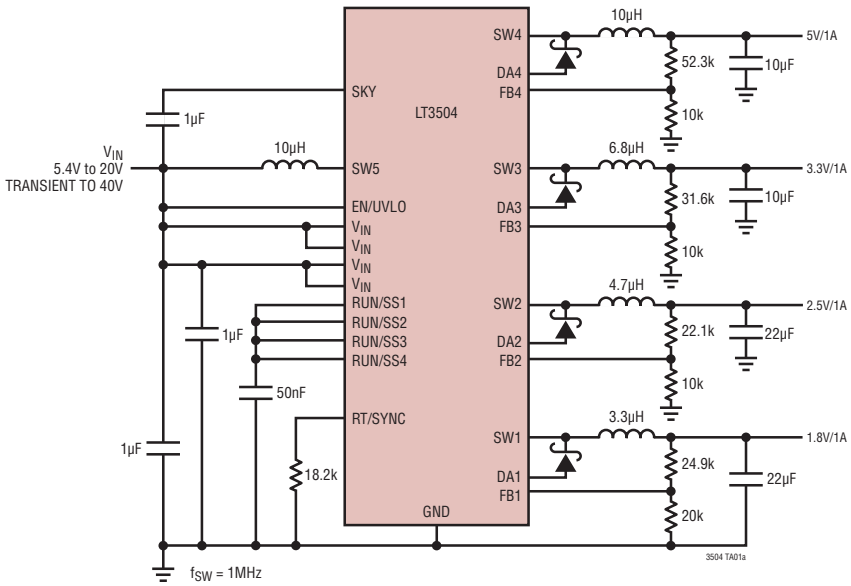
The LT®3504 consists of four 1A output current buck regulators. The LT3504 has a wide operating input range of 3.2V to 40V. An on-chip boost regulator allows each channel to operate up to 100% duty cycle and eliminates the need for four external charge pump circuits. The LT3504 is designed to minimize external component count and results in a simple and small application circuit.

The LT3504 operates robustly in fault conditions. Cycle-by-cycle peak current limit and catch diode current limit sensing protect the part during overload conditions. Thermal shutdown protects the power switches at elevated temperatures. Soft-start helps keep the peak inductor current under control during startup.

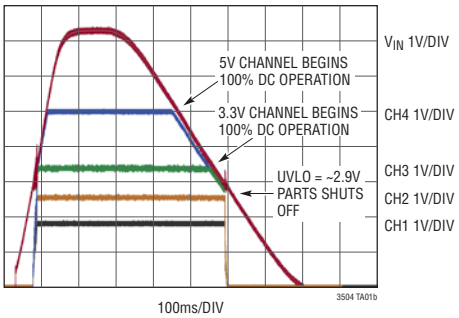
The LT3504 also features output voltage tracking and sequencing, programmable frequency, programmable undervoltage lockout, and a power good pin to indicate when all outputs are in regulation.

TYPICAL APPLICATION

Quad Buck Regulator in 4 × 5 QFN



LT3504 Start-Up and Shutdown Waveform. V_{IN} (Top Trace) Is Ramped from 0V Up to 8V and Then Back Down to 0V. The Other Four Traces Are the Output Voltages of All Four Channels

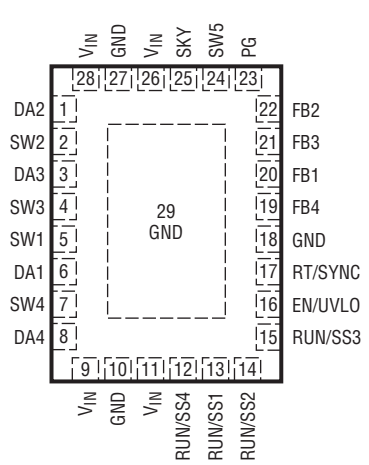


ABSOLUTE MAXIMUM RATINGS

(Note 1)

EN/UVLO Pin.....40V
EN/UVLO Pin Above V_{IN} Pin.....5V
V_{IN} Pin 40V
SKY Pin.....46V
SW5 Pin.....47V
RUN/SS Pins.....6V
FB Pins.....6V
RT/SYNC Pin.....6V
PG Pin.....25V
Operating Junction Temperature Range (Notes 2, 8)
LT3504EUFD ..... –40°C to 125°C
LT3504IUFD ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3504EUFD#PBF	LT3504EUFD#TRPBF	3504	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3504IUFD#PBF	LT3504IUFD#TRPBF	3504	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted.

SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EN/UVLO Threshold Voltage	Rising	●	1.2	1.44	1.6	V
EN/UVLO Threshold Voltage Hysteresis				110		mV
EN/UVLO Threshold Current Hysteresis	$V_{EN/UVLO}$ = Measured Rising Threshold – 50mV (Note 3)			1.3		µA
Internal V_{IN} Undervoltage Lockout			2.4	2.9	3.2	V
Quiescent Current (V_{IN}) in Shutdown	$V_{EN/UVLO}$ = 0V			0.01	2	µA
Quiescent Current (V_{IN})	$V_{EN/UVLO}$ = 1V (Note 4)			4	10	µA
Quiescent Current (V_{IN})	$V_{EN/UVLO}$ = 1.5V, $V_{RUN/SS(1,2,3,4)}$ = Open, $V_{FB(1,2,3,4)}$ = 0.9V, V_{SKY} = 17V			2.7		mA
Quiescent Current (SKY)	$V_{EN/UVLO}$ = 1.5V, $V_{RUN/SS(1,2,3,4)}$ = Open, $V_{FB(1,2,3,4)}$ = 0.9V, V_{SKY} = 17V			4.4		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted.

SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RUN/SS Pin Source Current	$V_{RUN/SS}$ = 0V			1.3		µA
RUN/SS Pin Threshold for Switching	V_{FB} = 0V		50	100		mV
Feedback Voltage		 ●	790 784	800 800	810 816	mV mV
FB Pin Current	V_{FB} = Measured V_{FB} (Note 5)	●		15	150	nA
Reference Line Regulation	V_{IN} = 5V to 40V			–0.015		%/V
SKY Pin Current	I_{SW} = 1A			27	40	mA
SKY Voltage above V_{IN} Voltage	$V_{SKY} – V_{IN}$			4.85		V
Switching Frequency	R_T = 6.34k R_T = 18.2k R_T = 100k	● ● ●	1.8 0.85 200	2.1 1 250	2.4 1.15 300	MHz MHz kHz
Switching Phase	R_T = 18.2k		150	180	210	Deg
SYNC Threshold Voltage				1.25		V
SYNC Input Frequency			0.35		2.2	MHz
Switch Current Limit (SW1,2,3,4)	(Note 6)		1.45	1.75	2.1	A
Switch V_{CESAT} (SW1,2,3,4)	I_{SW} = 1A			400		mV
Switch Leakage Current (SW1,2,3,4)				0.1	2	µA
Catch Diode Current Limit (SW1,2,3,4)	FB = 0V FB = 0.7V		0.75 1.0	1.15 1.45	1.33 1.67	A A
Switch Current Limit (SW5)	(Note 6)		220	320		mA
Switch V_{CESAT} (SW5)	I_{SW} = 200mA			230		mV
Switch Leakage Current (SW5)				0.1	2	µA
Boost Diode Current Limit (SW5)	V_{IN} = 5V		350	450		mA
PG Threshold Offset	V_{FB} Rising		65	90	125	mV
PG Hysteresis	V_{FB} Rising – V_{FB} Falling			35		mV
PG Voltage Output Low	I_{PG} = 250µA			180	300	mV
PG Pin Leakage	V_{PG} = 2V			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3504EUF is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3504IUF is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: Current flows into pin.

Note 4: Quiescent current (V_{IN}) is measured at $V_{EN/UVLO}$ = 1V

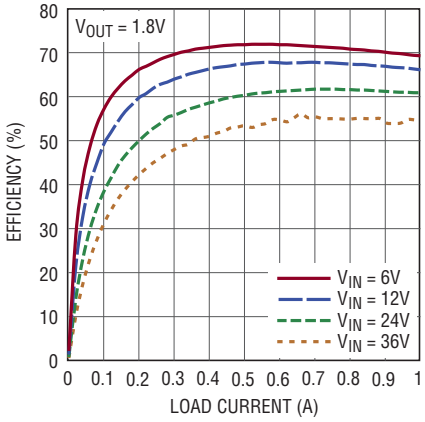
Note 5: Current flows out of pin.

Note 6: Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

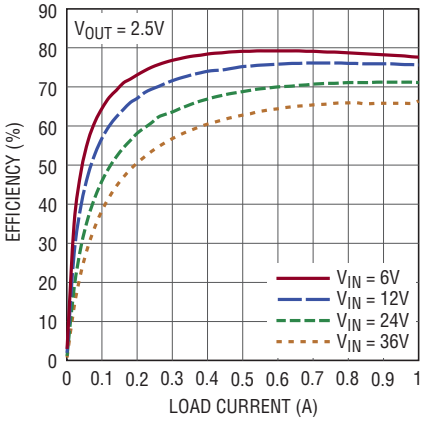
Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

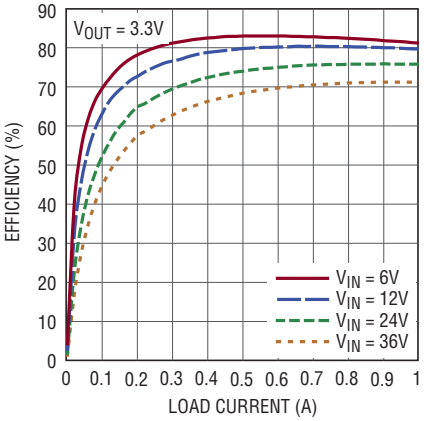
Efficiency, f = 1MHz



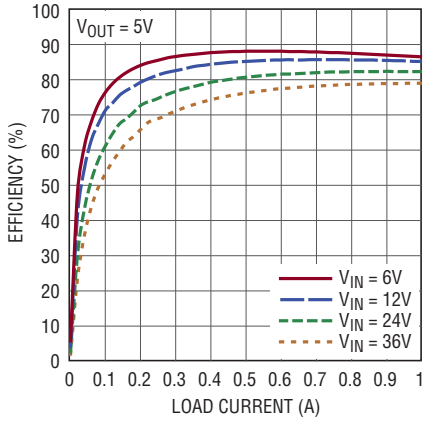
Efficiency, f = 1MHz



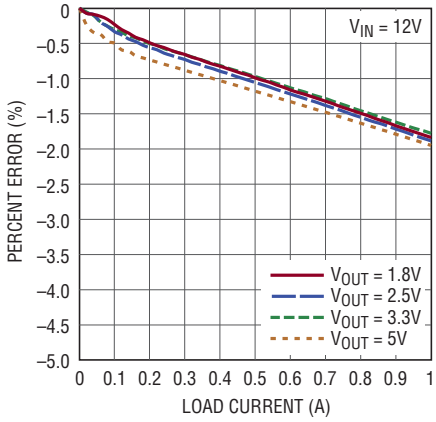
Efficiency, f = 1MHz



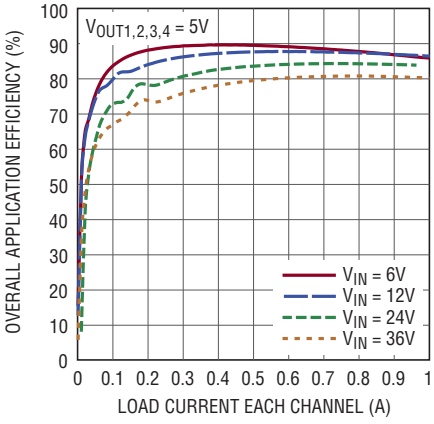
Efficiency, f = 1MHz



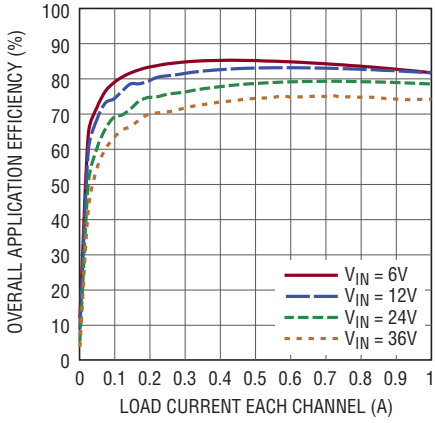
Load Regulation



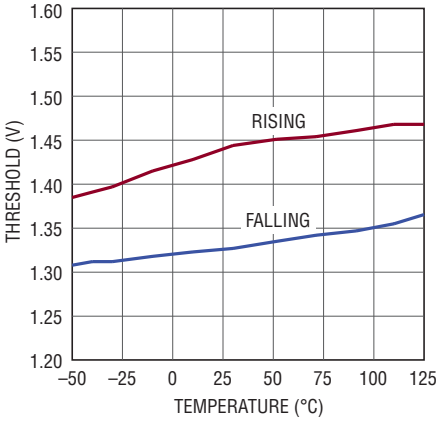
Efficiency, f = 1MHz



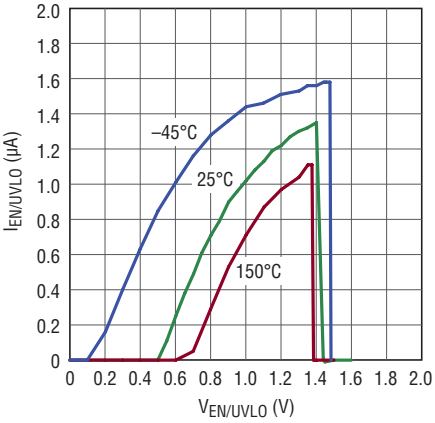
Efficiency 5V/3.3V/2.5V/1.8V, f = 1MHz



EN/UVLO Threshold



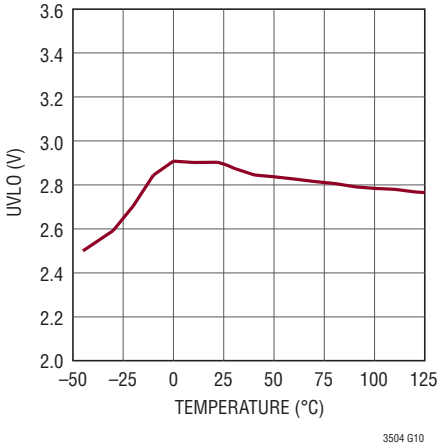
EN/UVLO Pin Current



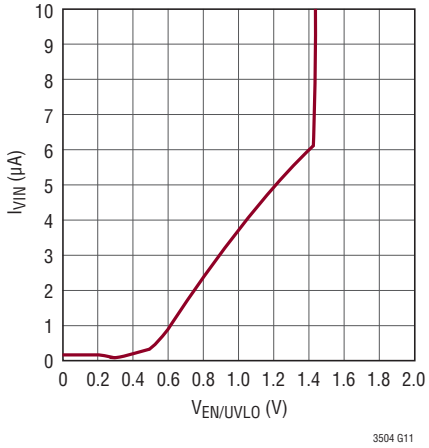
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

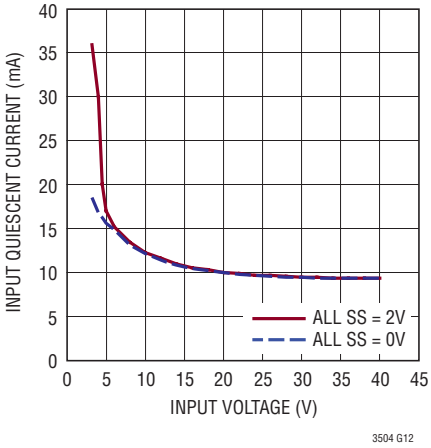
Input Voltage Undervoltage Lockout



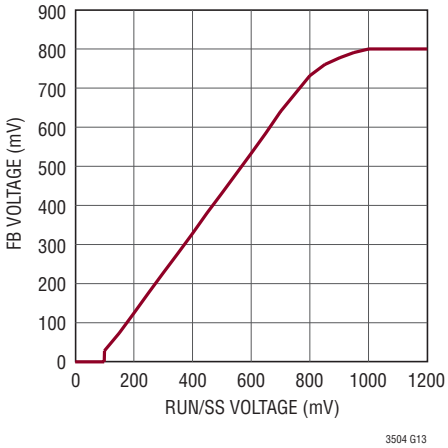
V_{IN} Pin Current



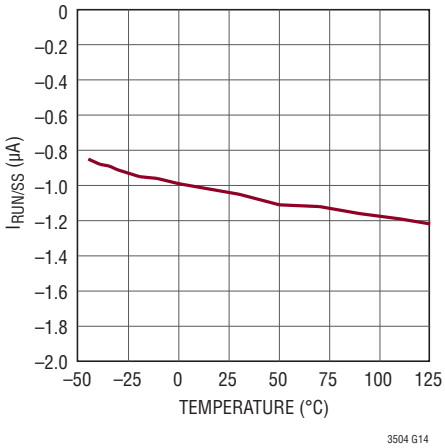
Input Quiescent Current vs Input Voltage



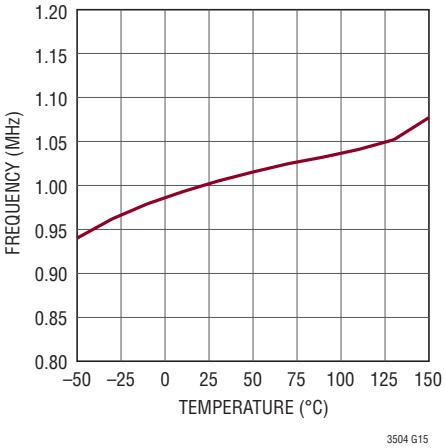
RUN/SS vs FB Voltage



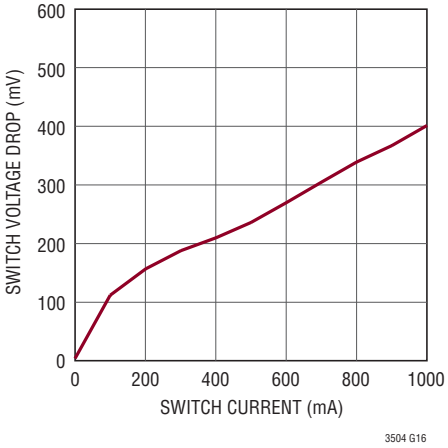
Soft Start Current



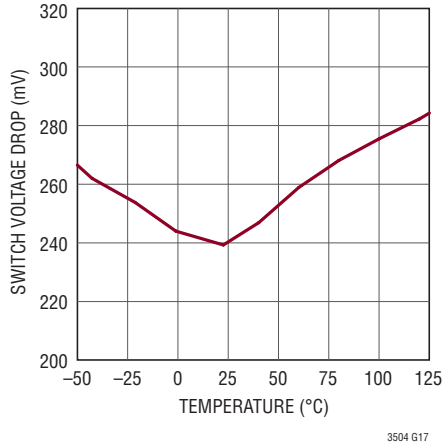
Switching Frequency vs Temperature



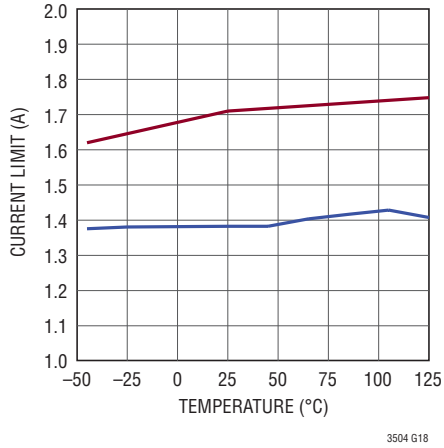
Switch Voltage Drop



Switch Voltage Drop, I_{SW} = 500mA

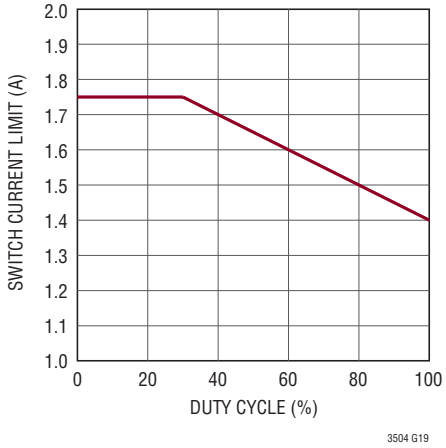


Switch and Diode Current Limit

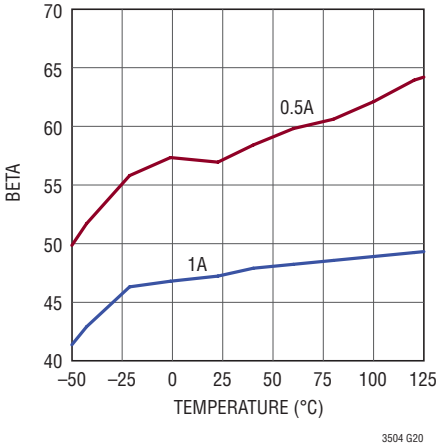


TYPICAL PERFORMANCE CHARACTERISTICS

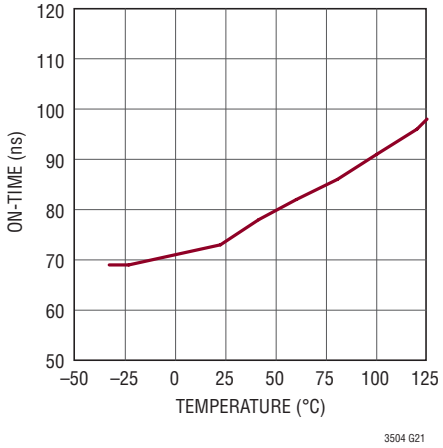
Switch Current Limit



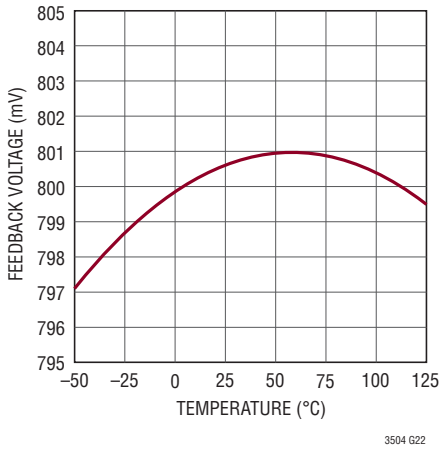
Switch Beta



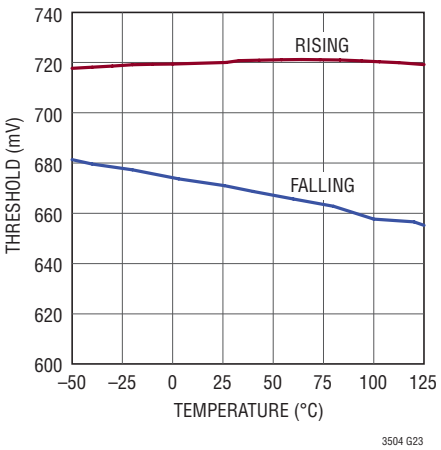
Minimum On-Time



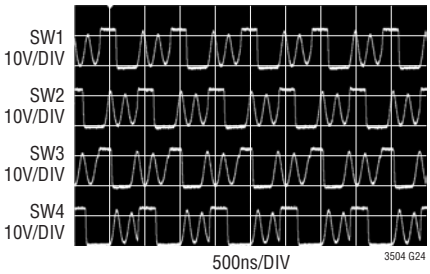
Feedback Voltage



Power Good Threshold

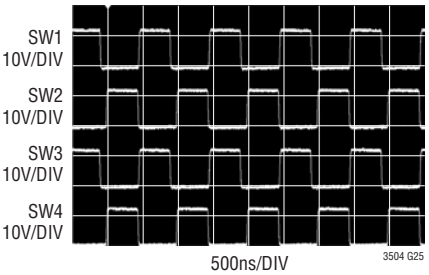


Operating Waveforms, Discontinuous Mode



$I_{OUT1,2,3,4}$ = 40mA
$V_{OUT1,2,3,4}$ = 5V

Operating Waveforms, Continuous Mode



$I_{OUT1,2,3,4}$ = 0.5A
$V_{OUT1,2,3,4}$ = 5V

PIN FUNCTIONS

DA (Pins 1, 3, 6, 8): Return the Schottky catch diode anode to the diode anode (DA) pin. An internal comparator senses the diode current and prevents switching when the diode current is higher than the DA pin current limit.

SW (Pins 2, 4, 5, 7): The SW pins are the output of the internal power switches. Connect each SW pin to an inductor and Schottky catch diode cathode.

V_{IN} (Pins 9, 11, 26, 28): The V_{IN} pins supply current to the LT3504's internal regulator and to the internal power switches. The V_{IN} pins should be tied together and locally bypassed with a capacitor to ground, preferably to pins 10 and 27.

GND (Pins 10, 18, 27, Exposed Pad Pin 29): Tie the GND pins to a local ground plane below the LT3504 and the circuit components. The exposed pad must be soldered to the PCB and electrically connected to ground. Use a large ground plane and thermal vias to optimize thermal performance.

RUN/SS (Pins 12, 13, 14, 15): The RUN/SS pins are used to soft start each channel and to allow each channel to track other outputs. Output tracking is implemented by connecting a resistor divider to this pin from the tracked output. For soft start, tie a capacitor from this pin to ground. An internal 1.3µA soft-start current charges the capacitor to create a voltage ramp at the pin. Each channel can be individually shut down by pulling RUN/SS below 0.1V.

EN/UVLO (Pin 16): The EN/UVLO pin is used to start up the internal regulator to power the reference and oscillator. It also starts up the internal boost regulator. Pull the EN/UVLO pin below 1.44V to shut down the LT3504. The LT3504 will draw less than 10µA of current from the V_{IN} pin when EN/UVLO is less than 1.44V. Pull EN/UVLO pin below 0.7V to put the LT3504 in a state where the part draws 0µA from the V_{IN} pin. The threshold can function as an accurate undervoltage lockout (UVLO), preventing the regulator from operating until the input voltage has reached the programmed level. Do not drive the EN/UVLO pin more than 5V above V_{IN}.

RT/SYNC (Pin 17): Set the switching frequency of the LT3504 by tying an external resistor from this pin to ground. Select the value of the programming resistor (R_T) according to Table 1 in the Applications Information section. The RT/SYNC pin is also used to synchronize the internal oscillator of the LT3504 to an external signal. The synchronization (sync) signal is directly logical compatible and can be driven by any signal with pulse width greater than 50ns. The synchronization range is from 250kHz to 2.2MHz.

FB (Pins 19, 20, 21, 22): Each feedback pin is regulated to 800mV. Connect the feedback resistor divider to this pin. The output voltage is programmed according to the following equation:

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{0.8V} - 1 \right)$$

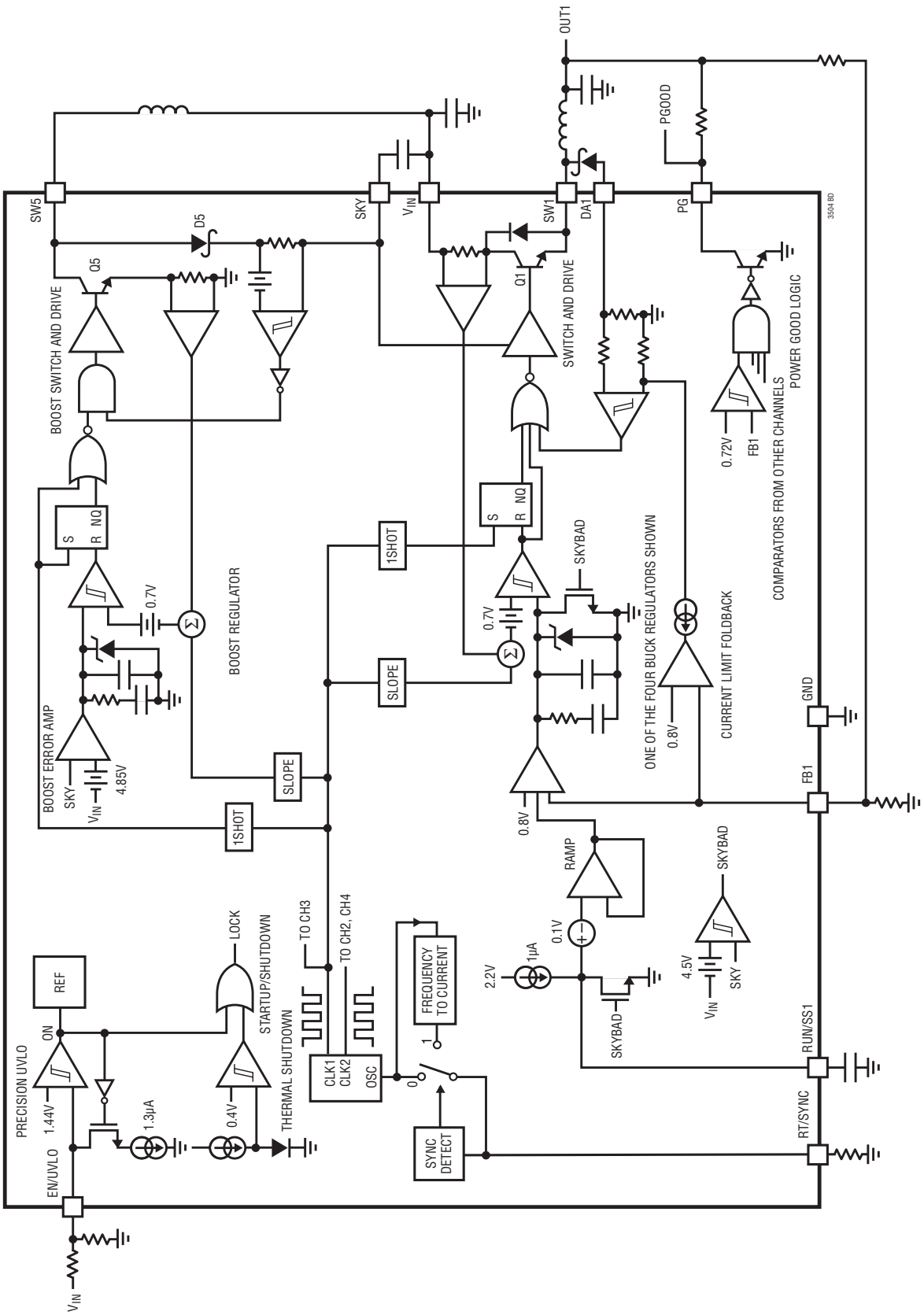
where R1 connects between OUT and FB, and R2 connects between FB and GND. A good value for R2 is 10kΩ.

PG (Pin 23): The Power Good pin is the open collector output of an internal comparator. PG remains low until all FB pins are greater than 710mV. If not in use, this pin can be left unconnected. The PG comparator is disabled in shutdown.

SW5 (Pin 24): The SW5 pin is an open collector of an internal boost regulator power switch. This power switch generates the drive voltage 4.85V above the input voltage (V_{IN}), to drive the internal buck regulator power switches. Connect an inductor from this pin to the V_{IN} pin.

SKY (Pin 25): The SKY pin is the output of an integrated power Schottky diode and is the source of drive voltage to the internal buck regulator power switches. Connect a 1µF capacitor from this pin to the V_{IN} pin. Do not drive this pin with an external voltage source. Do not draw current from this pin with an external component.

BLOCK DIAGRAM



OPERATION

A comparator starts the reference when the EN/UVLO pin rises above the 1.44V rising threshold. Other comparators prevent switching when the input voltage is below 2.9V or the die temperature is above 175°C. When the EN/UVLO is above 1.44V, the input voltage is above 3.2V, and the temperature is below 175°C, the boost regulator begins switching and charges the SKY capacitor to 4.85V above V_{IN}. When the SKY voltage is less than 4.5V above V_{IN}, the RUN/SS pins and V_C nodes are actively pulled low to prevent the buck regulators from switching.

The boost regulator (Channel 5) consists of an internal 0.4A power switch (Q5), an internal power Schottky diode (D5), and the necessary logic and other control circuitry to drive the switch. The switch current is monitored to enforce cycle-by-cycle current limit. The diode current is monitored to prevent inductor current runaway during transient conditions. An error amplifier servos the SKY voltage to 4.85V above V_{IN}. A comparator detects when the SKY voltage is 4.5V above V_{IN} and allows the buck regulators to begin switching.

The oscillator produces two antiphase clock signals running at 50% duty cycle. Channels 1, 3 and 5 run antiphase to Channels 2 and 4. The oscillator can be programmed by connecting a single resistor from RT/SYNC to ground, or by applying an external clock signal to RT/SYNC. A sync detect circuit distinguishes between the type of input. Tying a resistor to GND directly sets the bias current of the oscillator. The sync signal is converted to a current to set the bias current of the oscillator.

The oscillator enables an R_S flip-flop, turning on the internal 1.7A power switch Q1. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at the V_C node. A second comparator enforces a catch diode current limit to prevent inductor current runaway during transient conditions. An error amplifier measures the output voltage through an external resistor tied to the FB pin and servos the V_C node. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. A clamp on the V_C pin provides switch current limit. Each buck regulator switch driver operates by drawing current from the SKY pin. Regulating the SKY pin to 4.85V above the V_{IN} pin voltage is necessary to fully saturate the bipolar power switch for efficient operation.

Soft-start is implemented by generating a voltage ramp at the RUN/SS pin. An internal 1.3µA current source pulls the RUN/SS pin up to 2.1V. Connecting a capacitor from the RUN/SS pin to ground programs the rate of the voltage ramp on the RUN/SS pin. A voltage follower circuit with a 0.1V offset connected from the RUN/SS pin to the RAMP node prevents switching until the voltage at the RUN/SS pin increases above 0.1V. When the voltage at the RAMP node is less than 0.9V, the error amplifier servos the FB voltage to the RAMP node voltage. When the RAMP node voltage increases above 0.9V, then the error amplifier servos the FB voltage to 0.8V. Additionally, a current amplifier reduces the catch diode current limit when the FB voltage is below 0.8V to limit the inductor current during startup.

Each individual buck regulator can be placed in shutdown by pulling the respective RUN/SS pin below 0.1V. The EN/UVLO pin can be pulled low (below a V_{BE}) to place the entire part in shutdown, disconnecting the outputs and reducing the input current to less than 2µA.

The LT3504 is pin compatible with the 28-lead QFN package LT3514. The LT3514 is a three channel step-down converter and has one channel (CH3) that outputs 2A instead of 1A.

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FB Resistor Network

The output voltage is programmed with a resistor divider connected from the output and the FB pin. Choose the 1% resistor according to:

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{0.8V} - 1 \right)$$

A good value for R2 is 10kΩ, R2 should not exceed 20kΩ to avoid bias current error.

Input Voltage Range

The input voltage range for LT3504 applications depends on the output voltage and on the absolute maximum rating of the V_{IN} pin.

The minimum input voltage to regulate the output generally has to be at least 400mV greater than the greatest programmed output voltage. The only exception is when the largest programmed output voltage is less than 2.8V. In this case the minimum input voltage is 3.2V.

The absolute maximum input voltage of the LT3504 is 40V and the part will regulate output voltages as long as the input voltage remains less than or equal to 40V. However for constant-frequency operation (no pulse-skipping) the maximum input voltage is determined by the minimum on-time of the LT3504 and the programmed switching frequency. The minimum on-time is the shortest period of time that it takes the switch to turn on and off. Therefore the maximum input voltage to operate without pulse-skipping is:

$$V_{IN(PS)} = [\ (V_{OUT} + V_D)/(f_{SW} \bullet t_{ON(MIN)})\ ] + V_{SW} - V_D$$

where:

- $V_{IN(PS)}$ is the maximum input voltage to operate in constant frequency operation without skipping pulses.
- V_{OUT} is the programmed output voltage
- V_{SW} is the switch voltage drop, at I_{OUT} = 1A, V_{SW} = 0.4V
- V_D is the catch diode forward voltage drop, for an appropriately sized diode, V_D = 0.4V
- f_{SW} is the programmed switching frequency
- $t_{ON(MIN)}$ is the minimum on-time, worst-case over temperature = 110ns (at T = 125°C)

At input voltages that exceed $V_{IN(PS)}$ the part will continue to regulate the output voltage up to 40V. However the part will skip pulses (see Figure 1) resulting in unwanted harmonics, increased output voltage ripple, and increased peak inductor current. Provided that the inductor does not saturate and that the switch current remains below 2A, operation above $V_{IN(PS)}$ is safe and will not damage the part. For a more detailed discussion on minimum on-time and pulse-skipping, refer to the Applications Information section of the LT3505 data sheet.

Avoid starting up the LT3504 at input voltages greater than 36V, as the LT3504 must simultaneously conduct maximum currents at high V_{IN}. The maximum operating junction temperature of 125°C may be exceeded due to the high instantaneous power dissipation.

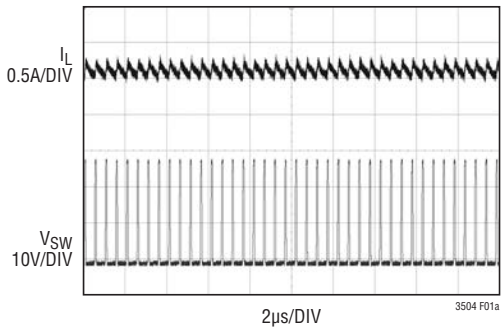

Figure 1a: The LT3504 Operating in Constant-Frequency Operation (Below $V_{IN(PS)}$), V_{IN} = 26.5V, V_{OUT} = 3.3V, f_{SW} = 2MHz, $t_{ON(MIN)}$ = 74ns at T = 25°C

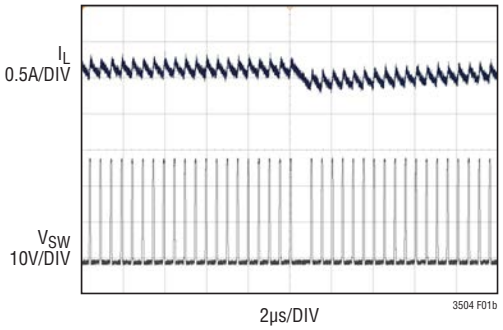

Figure 1b.The LT3504 Operating in Pulse-Skipping Mode (Above $V_{IN(PS)}$), V_{IN} = 27V, V_{OUT} = 3.3V, f_{SW} = 2MHz, $t_{ON(MIN)}$ = 74ns at T = 25°C

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Frequency Selection

The maximum frequency that the LT3504 can be programmed to is 2.5MHz. The minimum frequency is 250kHz. The switching frequency can be programmed in two ways. The first method is by tying a 1% resistor (R_T) from the RT/SYNC pin to ground. Table 1 can be used to select the value of R_T. The second method is to synchronize (sync) the internal oscillator to an external clock. The external clock must have a minimum amplitude from 0V to 1.6V and a minimum pulse-width of 50ns.

Table 1. RT/SYNC Pin Resistance to Program Oscillator Frequency

FREQUENCY (MHz)	RT/SYNC PIN RESISTANCE (kΩ)
0.20	140
0.3	82.5
0.4	56.2
0.5	43.2
0.6	34.8
0.7	28.0
0.8	23.7
0.9	20.5
1.0	18.2
1.1	16.9
1.2	14.7
1.3	13.0
1.4	11.5
1.5	10.7
1.6	9.76
1.7	8.66
1.8	8.06
1.9	7.32
2.0	6.81
2.1	6.34
2.2	6.04
2.3	5.62
2.4	5.36
2.5	4.99

In certain applications, the LT3504 may be required to be alive and switching for a period of time before it begins to receive a sync signal. If the sync signal is in a high impedance state when it is inactive then the solution is to simply tie an R_T resistor from the RT/SYNC pin to ground (Figure 2). The sync signal should be capable of driving the R_T resistor. If the sync signal is in a low impedance state or an unknown state when it is inactive, then the solution is to tie the R_T resistor from the RT/SYNC pin to ground and then to drive the RT/SYNC pin with the sync signal through a 1nF capacitor as shown in Figure 3.

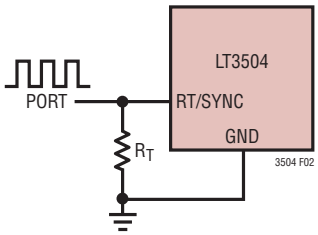

Figure 2. Driving the RT/SYNC Pin From a Port That Is in a High Impedance State When it Is Inactive

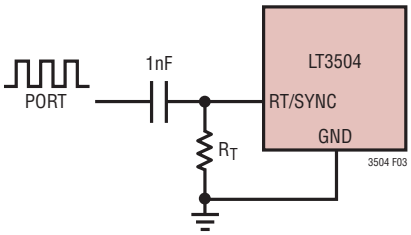

Figure 3. Driving the RT/SYNC Pin from a Port That Is in a Low Impedance State When it Is Inactive

BOOST Regulator and SKY Pin Considerations

The on-chip boost regulator generates the SKY voltage to be 4.85V above V_{IN}. The SKY voltage is the source of drive current for the buck regulators which is used to fully saturate the power switch. The boost regulator requires two external components: an inductor and a capacitor.

A good first choice for an inductor is given by:

$$L = \frac{20.5\mu H}{f}$$

where f is in MHz.

Thus, for a 250kHz programmed switching frequency, a good first choice for an inductor value is 82µH. For a 2.5MHz programmed switching frequency, a good first

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choice for an inductor value is 8.2µH. These values will ensure that each buck regulator will have sufficient drive current to saturate the power switch in all applications and under all operating conditions.

A user desiring a lower inductor current value can calculate their optimum inductor size based on their output current requirements. Each buck regulator instantaneously requires 20mA from the SKY pin per 1A of switch current. The average current that each buck regulator draws from the SKY pin is 20mA multiplied by the duty cycle. So if all four buck regulators run at 100% duty cycle with each channel supplying 1A of output current, then the SKY pin should be able to source 80mA. However if each channel runs at 50% duty cycle then the SKY pin only has to source 40mA. Alternatively if each channel runs at 100% duty cycle but the output current requirement is 0.5A per channel instead of 1A, then again the SKY pin only has to source 40mA. To summarize, the SKY pin output current requirement is calculated from the following equation:

$$I_{SKY} = \frac{\left(I_{OUT1} \bullet V_{OUT1} + I_{OUT2} \bullet V_{OUT2} + I_{OUT3} \bullet V_{OUT3} + I_{OUT4} \bullet V_{OUT4}\right)}{50 \bullet V_{IN}}$$

where I_{OUTX} is the desired output current from Channel X, V_{OUTX} is the programmed output voltage of Channel X, and V_{IN} is input voltage.

Once the SKY pin output current requirement is determined, the inductor value can be calculated based on the maximum tolerable inductor current ripple from the following equation:

$$L = \frac{V_{IN} \bullet DC5}{2 \bullet f_{SW} \bullet \left[0.3 \bullet \left(1 - 0.25 \bullet DC5\right) - I_{SKY}\right]}$$

where f_{SW} is the programmed switching frequency and DC5 is the boost regulator duty cycle, given by: DC5 = 5V/(V_{IN} + 5V).

For a 1MHz application, with V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V, V_{OUT3} = 2.5V, V_{OUT4} = 1.8V, and all channels supplying 1A of output current, the required SKY pin current is 21mA and the inductor value is 6µH.

Soft-Start/Tracking

The RUN/SS pin can be used to soft-start the corresponding channel, reducing the maximum input current during start-up. The RUN/SS pin is pulled up through a 1µA current source to about 2.1V. A capacitor can be tied to the pin to create a voltage ramp at this pin. The buck regulator will not switch while the RUN/SS pin voltage is less than 0.1V. As the RUN/SS pin voltage increases above 0.1V, the channel will begin switching and the FB pin voltage will track the RUN/SS pin voltage (offset by 0.1V), until the RUN/SS pin voltage is greater than 0.8V + 0.1V. At this point the output voltage will be at 100% of it's programmed value and the FB pin voltage will cease to track the RUN/SS pin voltage and remain at 0.8V (the RUN/SS pin will continue ramping up to about 2.1V with no effect on the output voltage). The ramp rate can be tailored so that the peak start up current can be reduced to the current that is required to regulate the output, with little overshoot. Figure 4 shows the start-up waveforms with and without a soft-start capacitor (C_{SS}) on the RUN/SS pin.

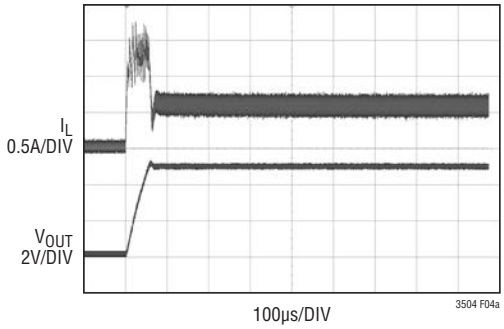

Figure 4a. Inductor Current Waveform During Start-Up without a Soft-Start Capacitor

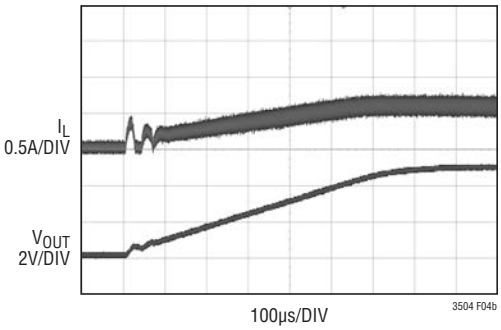

Figure 4b. Inductor Current Waveform During Start-Up with a 1nF Soft-Start Capacitor (C_{SS})

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Undervoltage Lockout

The LT3504 prevents switching when the input voltage decreases below 3.2V. Alternatively, the EN/UVLO pin can be used to program an undervoltage lockout at input voltages exceeding 3.2V by tapping a resistor divider from V_{IN} to EN/UVLO as shown in Figure 5.

The rising threshold on the EN/UVLO pin is 1.44V. The falling threshold on the EN/UVLO pin is 1.33V. When EN/UVLO is rising and less than 1.44V then the EN/UVLO pin sinks 1.3µA of current. This 1.3µA current can be used to program additional hysteresis on the EN/UVLO pin. For the circuit in Figure 5, R1 can be determined from:

$$R1 = \frac{V_{IN,HYSTERESIS} - \frac{0.11}{1.33}\left(V_{IN,FALLING}\right)}{1.3\mu A}$$

where $V_{IN,HYSTERESIS}$ is the desired amount of hysteresis on the input voltage and $V_{IN,FALLING}$ is the desired input voltage threshold at which the part will shut down. Notice that for a given falling threshold ($V_{IN,FALLING}$), the amount of hysteresis ($V_{IN,HYSTERESIS}$) must be at least:

$$V_{IN,HYSTERESIS} > \frac{0.11}{1.33} \bullet \left(V_{IN,FALLING}\right)$$

For a falling threshold of 10V, the minimum hysteresis is 0.827V. For a falling threshold of 30V, the minimum hysteresis is 2.48V.

R2 can be calculated once R1 is known:

$$R2 = R1 \bullet \frac{1.33}{V_{IN,FALLING} - 1.33}$$

The circuit shown in Figure 5 will start when the input voltage rises above 11V and will shutdown when the input voltage falls below 10V.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = 2 \bullet (V_{OUT} + V_D)/f_{SW}$$

where V_D is the voltage drop of the catch diode (~0.4V), L is in µH and f_{SW} is in MHz. With this value there will be no subharmonic oscillation for applications with 50% or greater duty cycle. The inductor's RMS current rating must be greater than your maximum load current and its saturation current should be about 30% higher. For robust operation in fault conditions, the saturation current should be above 2A. To keep efficiency high, the series resistance (DCR) should be less than 0.1Ω. Table 2 lists several vendors and types that are suitable.

Of course, such a simple design guide will not always result in the optimum inductor for your application. A larger value provides a higher maximum load current and reduces output voltage ripple at the expense of slower transient response. If your load is lower than 1A, then you can decrease the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Low inductance may result in discontinuous mode operation, which is okay, but further reduces maximum load current. For details on maximum output current and discontinuous mode operation, see Linear Technology Application Note 44.

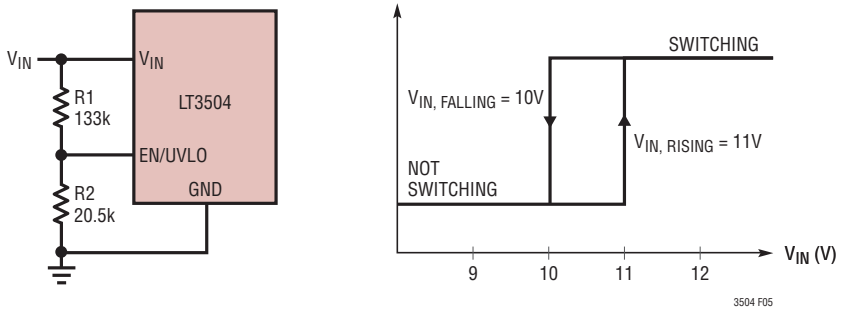

Figure 5. Circuit to Prevent Switching When V_{IN} < 10V, with 700mV of Hysteresis

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Table 2. Inductor Vendors

VENDOR	URL	PART SERIES	INDUCTANCE (µH)	SIZE (mm)
Sumida	www.sumida.com	CDRH4D28 CDRH5D28 CDRH5D28	1.2 TO 4.7 2.5 TO 10 2.5 TO 33	4.5 × 4.5 5.5 × 5.5 8.3 × 8.3
Toko	www.toko.com	A916CY D585LC	2 TO 12 1.1 TO 39	6.3 × 6.2 8.1 × 8
Würth Elektronik	www.we-online.com	WE-TPC(M) WE-PD2(M) WE-PD(S)	1 TO 10 2.2 TO 22 1 TO 27	4.8 × 4.8 5.2 × 5.8 7.3 × 7.3

Table 3. Capacitor Vendors

VENDOR	PHONE	URL	PART SERIES	COMMENTS
Panasonic	(714) 373-7366	www.panasonic.com	Ceramic, Polymer, Tantalum	EEF Series
Kemet	(864) 963-6300	www.kemet.com	Ceramic, Tantalum	T494, T495
Sanyo	(408) 749-9714	www.sanyovideo.com	Ceramic, Polymer, Tantalum	POSCAP
Murata	(404) 436-1300	www.murata.com	Ceramic	
AVX		www.avxcorp.com	Ceramic, Tantalum	TPS Series
Taiyo Yuden	(864) 963-6300	www.taiyo-yuden.com	Ceramic	

Catch Diode

Use a 1A Schottky diode. The diode must have a reverse voltage rating equal to or greater than the maximum input voltage. The ON Semiconductor MBRM140 is a good choice; it is rated for 1A continuous forward current and a maximum reverse voltage of 40V.

Input Capacitor

The input of the LT3504 circuit must be bypassed with a X7R or X5R type ceramic capacitor. Y5V types have poor performance over temperature and amplified voltage and should not be used. There are four V_{IN} pins. Each V_{IN} pin should be bypassed to the nearest ground pin. However it is not necessary to use a dedicated capacitor for each V_{IN} pin. Pins 9 and 11 may be tied together on the board layout so that both pins can share a single bypass capacitor. Since the channels running on Pins 9 and 11 are 180 degrees out-of-phase, it is not necessary to double the capacitor value either. Similarly, Pins 26 and 28 may be tied together on the board layout to save a bypass capacitor. For switching frequencies greater than 750kHz, a 1µF capacitor or higher value ceramic capacitor should be used to bypass each group of two V_{IN} pins. For switching frequencies less than 750kHz, a 2.2µF or higher value ceramic capacitor should be used to bypass each group of two V_{IN} pins. The ceramic bypass capacitors should be located as close to the V_{IN} pins as possible. See the sample layout shown in the PCB Layout section. All four V_{IN} pins should be tied together on the board and bypassing with a low performance electrolytic capacitor is recommended especially if the input power source has high impedance, or there is significant inductance due to long wires or cables.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3504 and to force this very high frequency switching current into a tight local loop, minimizing EMI. To accomplish this task, the input bypass capacitor must be placed close to the LT3504 and the catch diode; see the PCB Layout section. A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3504. A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT3504 circuit is plugged into a live supply, the input voltage can ring to

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twice its nominal value, possibly exceeding the LT3504's voltage rating. This situation can be easily avoided by adding an electrolytic capacitor in parallel with the ceramic input capacitors. See Application Note 88.

Output Capacitor

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3504 to produce the DC output. In this role it determines the output ripple so low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3504's control loop.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good value is:

$$C_{OUT} = 33/(V_{OUT} \bullet f_{SW})$$

where C_{OUT} is in µF and f_{SW} is in MHz. Use X5R or X7R types and keep in mind that a ceramic capacitor biased with V_{OUT} will have less than its nominal capacitance. This choice will provide low output ripple and good transient response. Transient performance can be improved with a high value capacitor, if the compensation network is also adjusted to maintain the loop bandwidth.

A lower value of output capacitor can be used, but transient performance will suffer.

High performance electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier and should be 0.1Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance, because the capacitor must be large to achieve low ESR. Table 3 lists several capacitor vendors.

Figure 6 shows the transient response of the LT3504 with several output capacitor choices. The output is 3.3V. The load current is stepped from 500mA to 1A and back to 500mA and the oscilloscope traces show the output voltage. The upper photo shows the recommended value. The second photo shows the improved response (less voltage drop) resulting from a larger output capacitor and a larger phase lead capacitor. The last photo shows the response to a high performance electrolytic capacitor. Transient performance is improved due to the large output capacitance.

Shorted and Reversed Input Protection

If the inductor is chosen so that it won't saturate excessively, an LT3504 buck regulator will tolerate a shorted output. There is another situation to consider in systems where the output will be held high when the input to the LT3504 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LT3504's output. If the V_{IN} pin is allowed to float and the EN/UVLO pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3504's internal circuitry will pull its quiescent current through its SW pin. This is fine if your system can tolerate a few mA in this state. If you ground the EN/UVLO pin, the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3504 can pull large currents from the output through the SW pin and the V_{IN} pin. Figure 7 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

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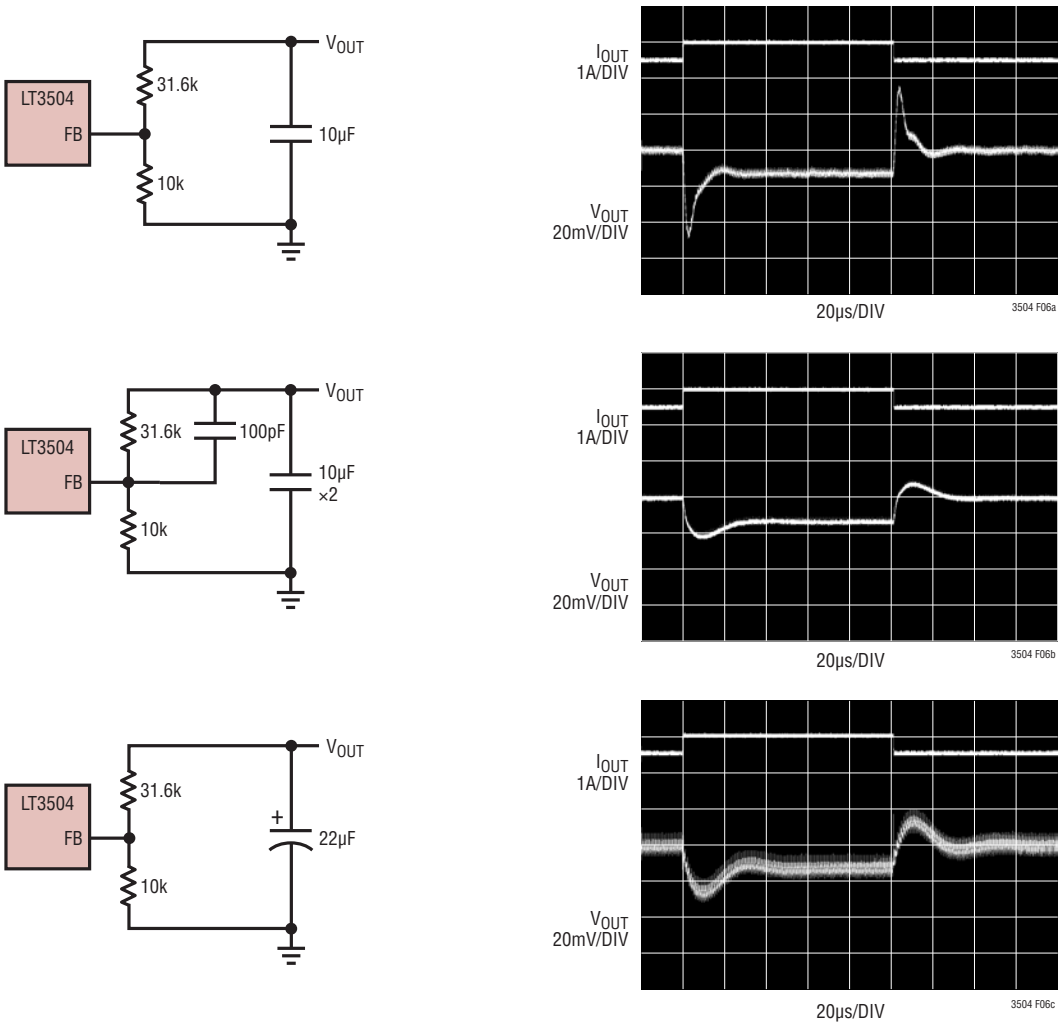

Figure 6. Transient Load Response of the LT3504 with Different Output Capacitors as the Load Current Is Stepped from 500mA to 1A. V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_T = 18.2k

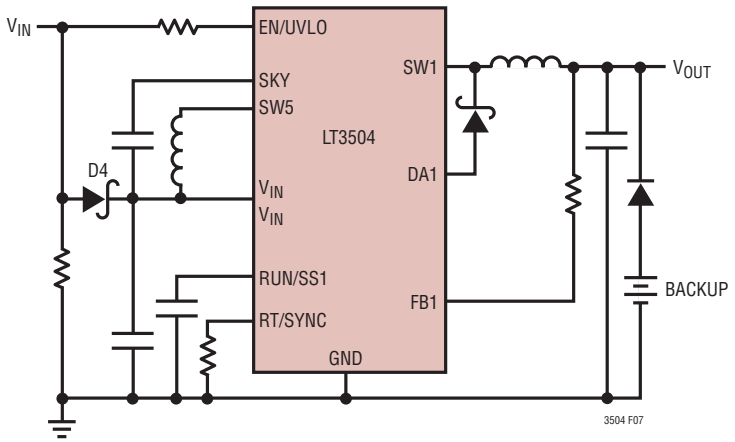

Figure 7. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output; It Also Protects the Circuit from a Reversed Input. The LT3504 Runs Only When the Input Is Present

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PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 8 shows the recommended component placement with trace, ground plane, and via locations.

Note that large, switched currents flow in the LT3504's V_{IN}, SW and DA pins, the catch diodes (D1, D2, D3, D4) and the input capacitors (C5, C6). The loop formed by these components should be as small as possible and tied to system ground in only one place. These components, along with the inductors (L1, L2, L3, L4, L5) and output capacitors (C1, C2, C3, C4, C7), should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components, and tie this ground plane to system ground at one location (ideally at the ground terminal of the output capacitors). Ground pins (Pins 10, 27) are provided near the V_{IN} pins so that the V_{IN} pins can be bypassed to these ground pins. The SW nodes should be kept as small as possible and kept far away from the RT/SYNC and FB nodes. Keep the RT/SYNC node and FB nodes small so that the ground pin and ground traces will shield them from the SW nodes. If the user plans on using a SYNC signal to set the oscillator frequency then the RT/SYNC node should be kept away from the FB nodes. Include vias near the exposed pad of the LT3504 to help transfer heat from the LT3504 to the ground plane. Keep the SW5 pad/trace as far away from the FB pads as possible.

High Temperature Considerations

While the LT3504 is capable of delivering total output current up to 4A, total power dissipation for an application circuit and the resulting temperature rise must be considered, especially if all four channels are operating at high duty cycle.

The die temperature of the LT3504 must be lower than the maximum rating of 125°C. This is generally not a concern unless the ambient temperature is above 85°C. For higher temperatures, extra care should be taken in the layout of the circuit to ensure good heat sinking of the LT3504. The maximum load current should be derated as the ambient temperature approaches 125°C. Programming the LT3504 to a lower switching frequency will improve efficiency and reduce the dependence of efficiency on input voltage. The die temperature is calculated by multiplying the LT3504 power dissipation by the thermal resistance from junction to ambient. Power dissipation within the LT3504 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode losses. Thermal resistance depends on the layout of the circuit board, but 43°C/W is typical for the QFN package. Thermal shutdown will turn off the buck regulators and the boost regulator when the die temperature exceeds 175°C, but this is not a warrant to allow operation at die temperatures exceeding 125°C.

Outputs Greater Than 9V

For outputs greater than 9V, add a 1k resistor in series with a 1nF capacitor across the inductor to damp the discontinuous ringing of the SW node, preventing unintended SW current. An application with a 15V output (back page) shows the location of this damping network.

Other Linear Technology Publications

Application Notes 19, 35, 44 contain more detailed descriptions and design information for step-down regulators and other switching regulators. Design Note 318 shows how to generate a bipolar output supply using a step-down regulator.

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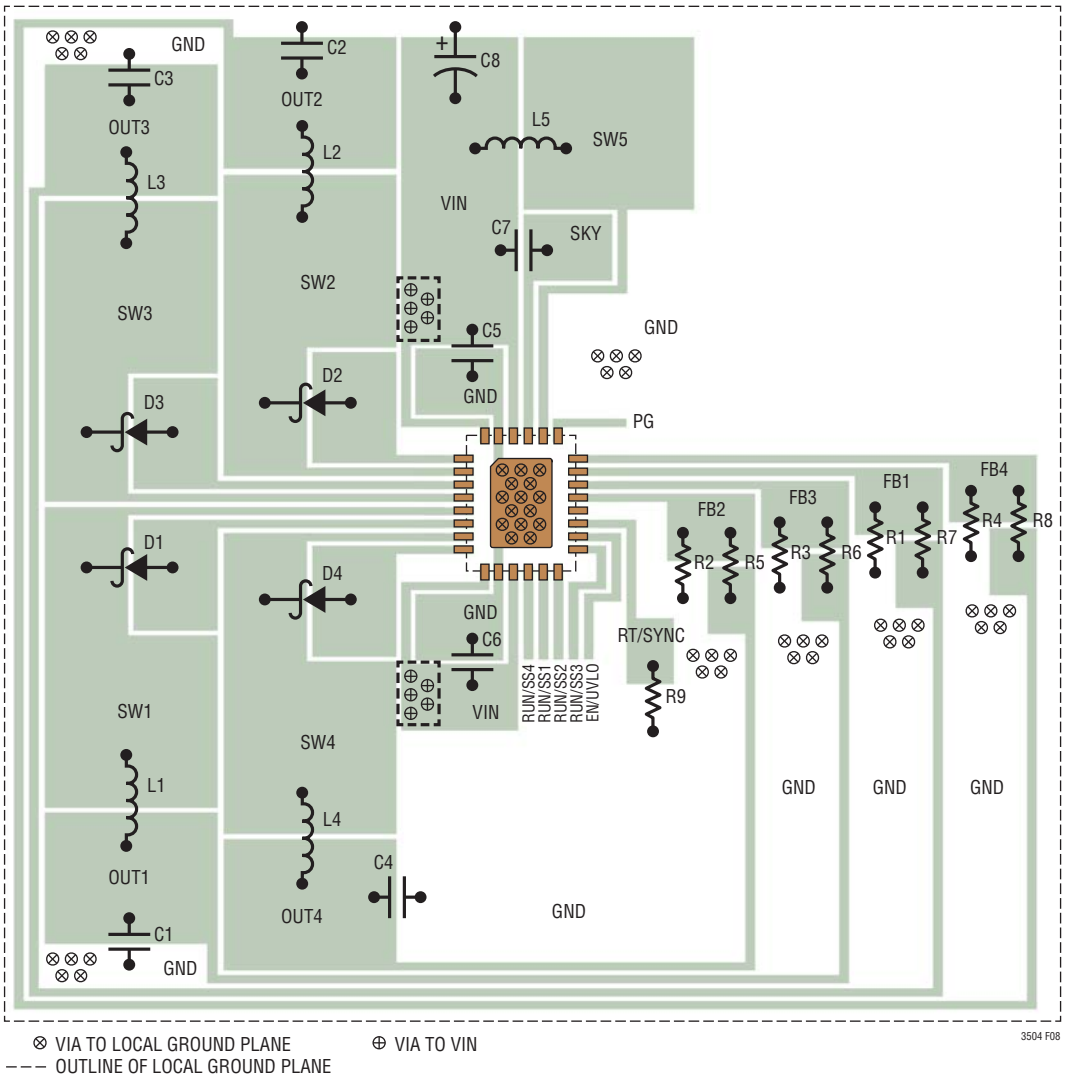

Figure 8

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Overvoltage Transient Protection

Figure 9 shows the complete application circuit for a 4-output step-down regulator with 100% duty cycle operation that withstands 180V surges. Under normal operating conditions (V_{IN} < 33V), the V_{SKY} rail supplies gate drive to MOSFET Q1, providing the LT3504 with a low resistance path to V_{SUPPLY}. In the event that a supply surge occurs, Zener diode D1 clamps Q1's gate voltage to 36V. The source-follower configuration prevents V_{IN} from rising any further than about 33V (a V_{GS} below the Zener clamp voltage). Figure 10 shows the LT3504 regulating all four channels through a 180V surge event without interruption.

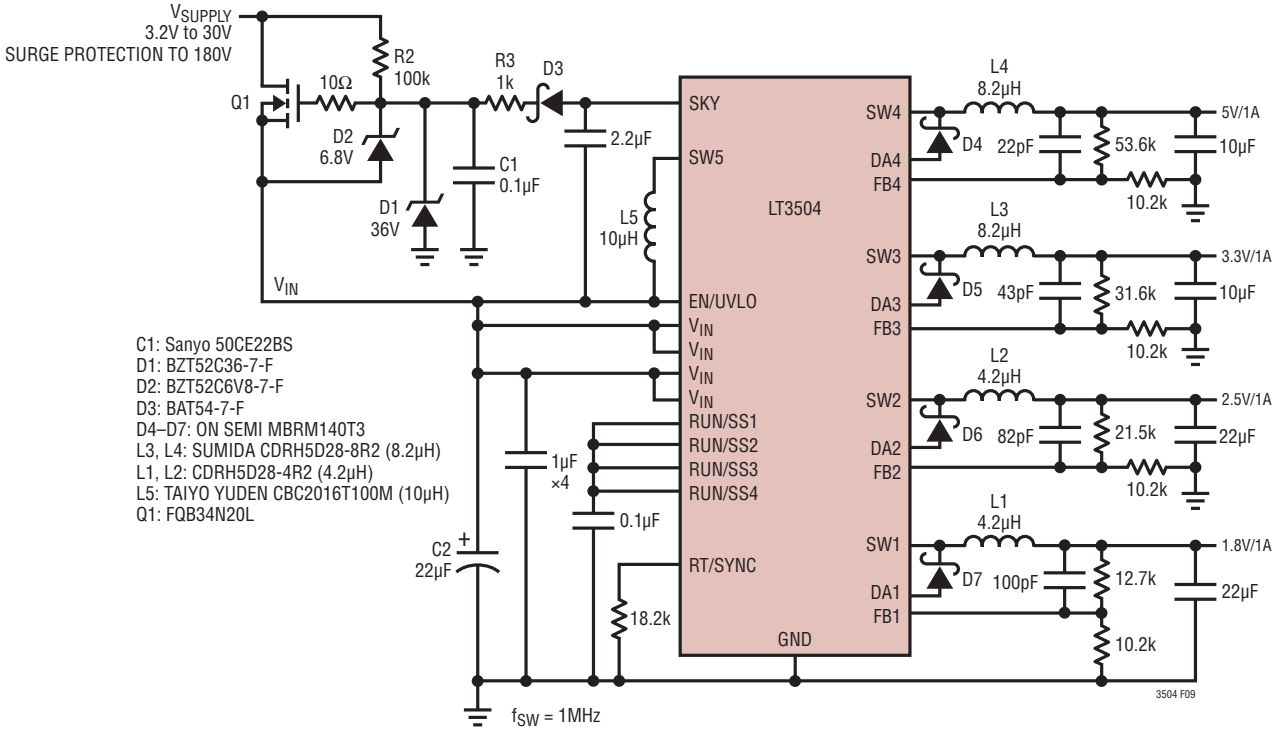


Figure 9. Complete Quad Buck Regulator with 180V Surge Protection

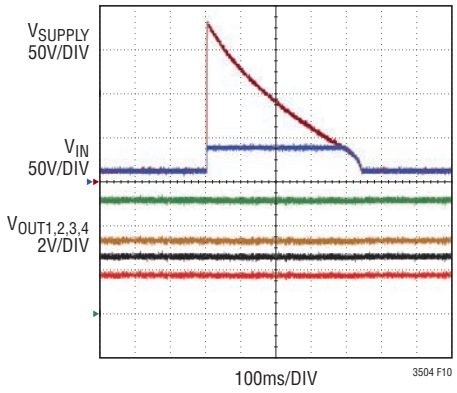


Figure 10. Overvoltage Protection Withstands 180V Surge

APPLICATIONS INFORMATION

Bear in mind that significant power dissipation occurs in Q1 during an overvoltage event. The MOSFET junction temperature must be kept below its absolute maximum rating. For the overvoltage transient shown in Figure 10, MOSFET Q1 conducts 0.5A (full load on all buck channels) while withstanding the voltage difference between V_{SUPPLY} (180V peak) and V_{IN} (33V). This results in a peak power of 74W. Since the overvoltage pulse in Figure 10 is roughly triangular, average power dissipation during the transient event (about 400ms) is approximately half the peak power. As such, the average power is given by:

$$P_{AVG}(W) = \frac{1}{2} \bullet P_{PEAK}(W) = 37W$$

In order to approximate the MOSFET junction temperature rise from an overvoltage transient, one must determine the MOSFET transient thermal response as well as the MOSFET power dissipation. Fortunately, most MOSFET transient thermal response curves are provided by the manufacturer (as shown in Figure 11). For a 400ms pulse duration, the FQB34N20L MOSFET thermal response $Z_{\Theta JC}(t)$ is 0.65°C/W. The MOSFET junction temperature rise is given by:

$$T_{RISE}(°C) = Z_{\theta JC}(t) \bullet P_{AVG}(W) = 24°C$$

Note that, by properly selecting MOSFET Q1, it is possible to withstand even higher input voltage surges. Consult manufacturer data sheets to ensure that the MOSFET operates within its Maximum Safe Operating Area.

The application circuit start-up behavior is shown in Figure 12. Resistor R2 pulls up on the gate of Q1, forcing source-connected V_{IN} to follow approximately 3V below V_{SUPPLY}. Once V_{IN} reaches the LT3504's 3.2V minimum start-up voltage, the on-chip boost converter immediately regulates the V_{SKY} rail 4.85V above V_{IN}. Diode D3 and resistor R3 bootstrap Q1's gate voltage to the V_{SKY}, fully enhancing Q1. This connects V_{IN} directly to V_{SUPPLY} through Q1's low resistance drain-source path. It should be noted that, prior to V_{SKY} being present, the minimum input voltage is about 6.2V. However, with V_{SKY} in regulation and Q1 enhanced, the minimum run voltage drops to 3.2V, permitting the LT3504 to maintain regulation through deep input voltage dips Figure 13 shows all channels operating down to the LT3504's 3.2V minimum input voltage.

APPLICATIONS INFORMATION

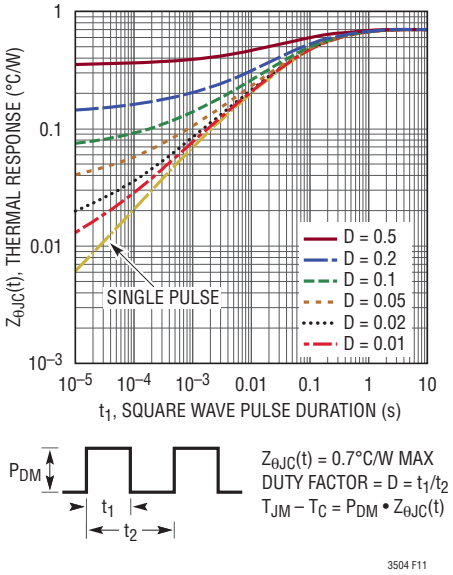


Figure 11. FQB34N20L Transient Thermal Response

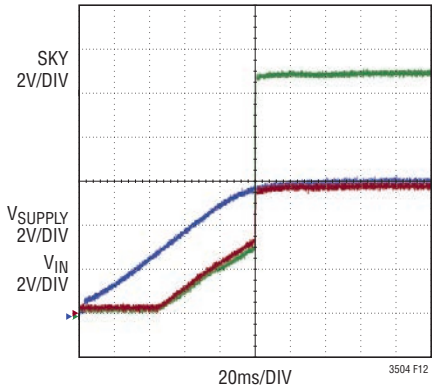


Figure 12. Figure 9's Start-Up Behavior

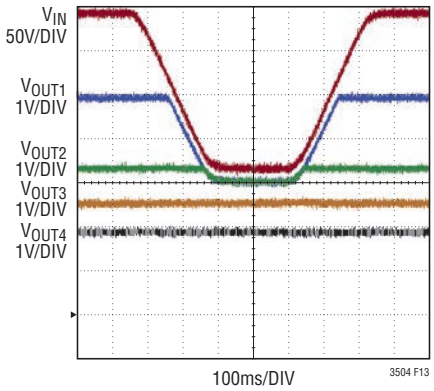
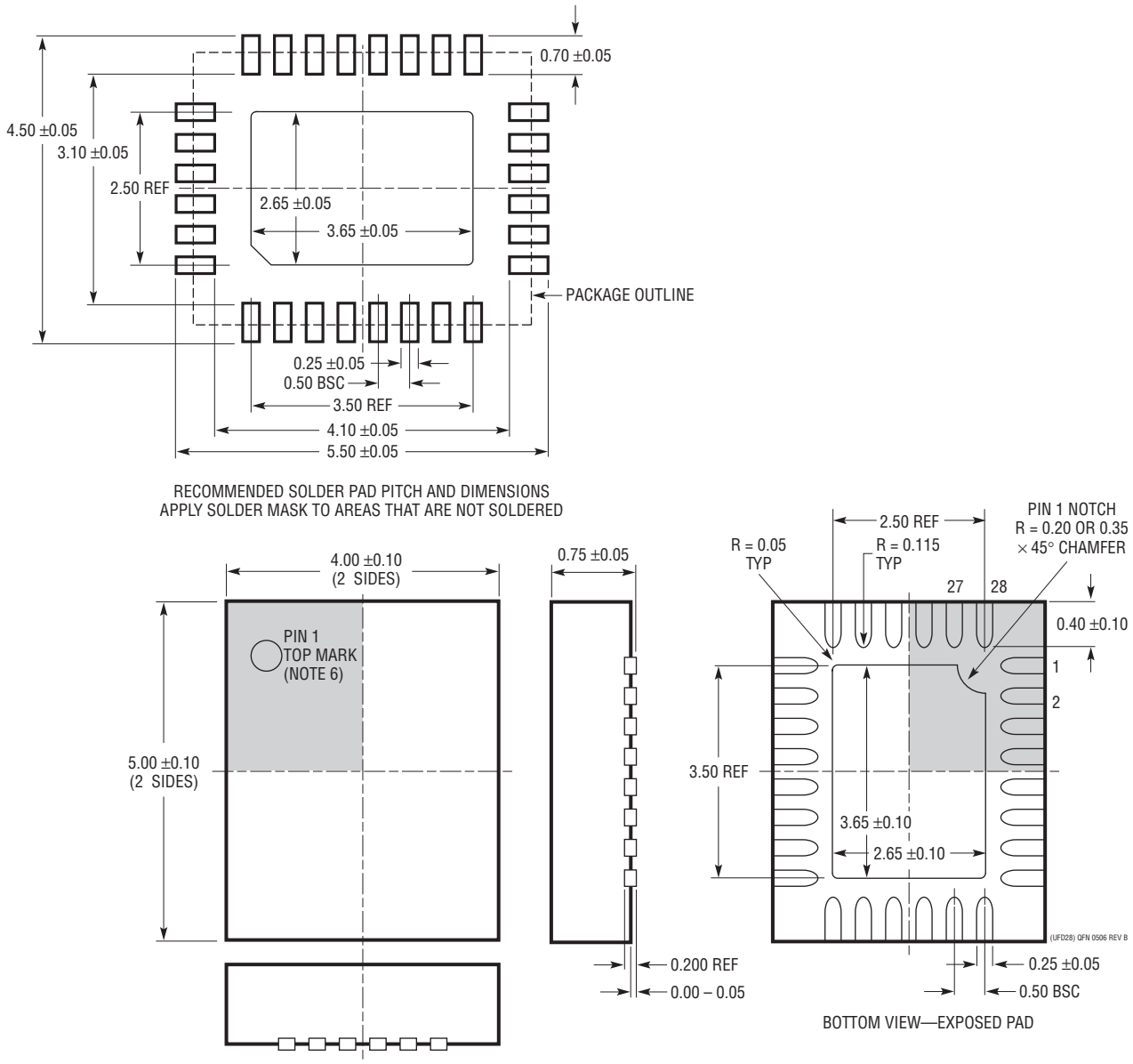


Figure 13. Figure 9's Dropout Performance

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



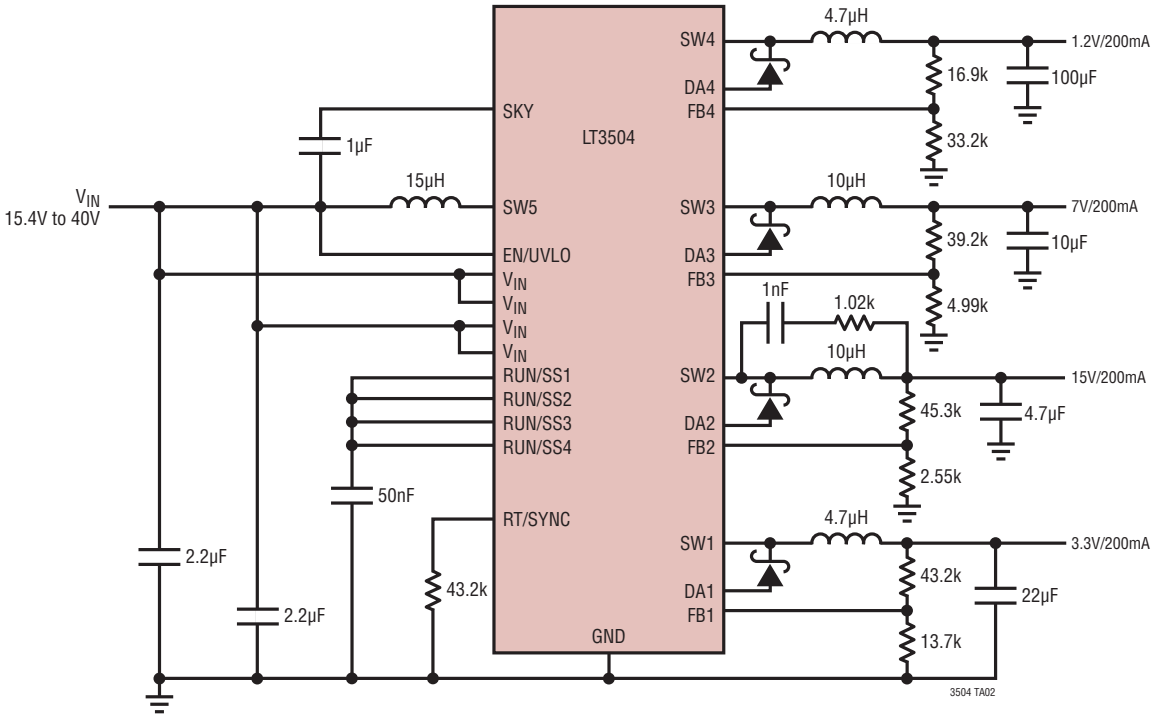
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/13	Clarified the minimum SYNC range.	1
		Clarified the parameters in the Electrical Characteristics section.	3
		Added the Input Quiescent Current vs Input Voltage graph.	5
		Clarified SKY capacitor maximum voltage.	9
		Clarified the Applications Information section.	10, 11, 12, 13, 17, 18

TYPICAL APPLICATION

40V Quad Output Application at 500kHz



RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT3507/ LT3507A	36V 2.5MHz, Triple [2.4A + 1.5A + 1.5A (I_{OUT})] with LDO Controller High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 4V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7mA, I_{SD} = 1µA, 5mm x 7mm QFN-38 Package
LT8610	42V 2.2MHz, Synchronous, Low I_Q = 2.5µA, Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} = 1µA, MSOP-16E Package
LT3988	60V with Transient Protection to 80V, 2.5MHz, Dual 1A High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 4.0V, $V_{IN(MAX)}$ = 60V, $V_{OUT(MIN)}$ = 0.75V, I_Q = 2mA, I_{SD} = 1µA, MSOP-16E Package
LT3509	36V with Transient Protection to 60V, Dual 0.70(I_{OUT}), 2.2MHz, High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} = 1µA, 3mm × 4mm DFN-14, MSOP-16E Packages
LT3500	36V, 40V_{MAX}, 2A, 2.5MHz High Efficiency Step-Down DC/DC Converter and LDO Controller	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} <10µA, 3mm × 3mm DFN-10 Package
LT3508	36V with Transient Protection to 40V, Dual 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.7V, $V_{IN(MAX)}$ = 37V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 4.6mA, I_{SD} = 1µA, 4mm × 4mm QFN-24, TSSOP-16E Packages
LT3980	58V with Transient Protection to 80V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 58V, Transient to 80V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 85µA, I_{SD} <1µA, 3mm × 4mm DFN-16 and MSOP-16E Packages
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} <1µA, 3mm × 3mm DFN-10, MSOP-10E Packages
LT3689	36V, 60V Transient Protection, 800mA, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter with POR Reset and Watchdog Timer	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, Transient to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} <1µA. 3mm × 3mm QFN-16 Package
LT3970	40V, 350mA, 2MHz High Efficiency Micropower Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 4V, $V_{IN(MAX)}$ = 40V, Transient to 60V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2µA, I_{SD} <1µA, 3mm × 2mm DFN-10 and MSOP-10 Packages
LT3682	36V, 60VMAX, 1A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 3mm DFN-12 Package

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